REMARKS

Claims 1-28 are in the application of which claims 1, 14, and 22 are in independent form.

An appendix is provided to show a marked up version of changes to the specification.

The disclosure is objected to because the number "40" should be changed to "50" on line 19 of page 5. It is believed that page 7 was intended. The paragraph containing this error is amended to correct it.

Applicants thank the Examiner for noticing this error.

Claim 13 stands rejected under 35 U.S.C. § 112, ¶ 1, for not meeting the written description requirement. Claim 13 is part of the original disclosure. Therefore, it is not new matter to add paragraph to the specification stating what claim 13 says. Such a pargraph is added following the paragraph ending at page 11, line 29. With this amendment, the requirements of 35 U.S.C. § 112 are met.

Claims 1, 4, 8-14, 17, 21-22, and 25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over admitted prior art (FIG. 1 and FIG. 9) and Patent 5,883,423 to Patwa (hereinafter "Patwa").

The Office action, p. 3, states: "Amitted prior art does not disclose the semiconductor capacitor operating in depletion mode ..." and "Patwa does not disclose the semiconductor capacitor operating in depletion mode ...." (Emphasis added.)

Independent claims 1 and 14 each recite that the "capacitor is in depletion mode ...." The Office action presents no evidence that it would be obvious to operate the prior art capacitors in depletion mode, but rather just says it would be obvious. In the absense of evidence, the rejection is improper and should be withdrawn.

Claim 22 states "the semiconductor capacitor having a flatband voltage and wherein the power supply voltage has a smaller absolute value than does the flatband voltage."

The Office action, p. 7, states with reference to the amitted prior art: "the semiconductor capacitor having a flatband voltage (page 6, line 25) but does not teach the power supply voltage has a smaller absolute value than does the flatband voltage." (Emphasis added.) The Office action, p. 7, does not provide evidence that it would be obvious, but rather merely asserts:

"it is well known as shown in FIG. 3 and conventional to have this voltage in order to obtain depletion mode. Therefore, it would be obvious to one having ordinary skill in the art at

the time the invention was made to apply this power since it is required to have small voltage than flatband voltage to obtain depletion mode." (Emphasis added.)

This is merely an assertion, not evidence. As shown above from the quotes from the Office action, the Office action presents no evidence of using the semiconductor capacitor in depletion mode. Therefore, that a particular voltage is desirable to obtain depletion mode is not evidence that "the power supply voltage has a smaller absolute value than does the flatband voltage." Accordingly, the rejection of claim 22 should be withdrawn.

Claims 4, 8-13, 17, 21, and 25 are dependent on one of independent claims 1, 14, or 22 and would also be patented.

Claims 2-3, 7, 15-16, 20, 23-24, and 28 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over admitted prior art (FIG. 9) and Patent 5,032,892 to Chern et al. Claims 2-3, 7, 15-16, 20, 23-24, and 28 are each dependent on one of independent claims 1, 14, or 22 and would also be patented.

Claims 5-6, 18-19, and 26-27 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over admitted prior art (FIG. 1) and Patent 5,032,892 to Chern et al. Claims 5-6, 18-19, and 26-27 are each dependent on one of independent claims 1, 14, or 22 and would also be patented.

Note that merely because applicants do not specifically argue that certain limitations of a claim are not in the references is not a concession that a reference or combination of references includes the limitations. That applicants do not contradict a particular statement made in the Office action is not a concession that applicants agree with it. Further, merely because applicants do not separately argue the patentability of every dependent claim is not a concession that there are not additional reasons for patentability of these dependent claims.

Applicants believe the application is in condition for allowance and respectfully request the same.

Respectfully submitted,

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APPENDIX:

IN THE SPECIFICATION (versions with markings to shown changes made)

Please substitute the following paragraph (including amendments to lines 19 and 23 of page 7) for the paragraph which is on page 7, from lines 18 to 29:

"FIG. 5 illustrates MOS-C 50 according to some embodiments of the invention. MOS-C [40] 50 is designated p+/n+ on n-body, according to the above described nomenclature. Vg is Vcc and S/D/B are at 0 (Vss). The curve of FIG. 3 will apply because an n-well is used and the poly and body have a different type. V_{FB} of MOS-C 50 is approximately 1V. V_{GB} = Vcc. If Vcc > V_{FB}, then MOS-C 50 is in the accumulation mode (channel accumulates) and if MOS-C < V_{FB}, then MOS-C [40] 50 is in the depletion mode (channel depletes). When Vcc = V_{FB}, the mode is between accumulation and depletion mode. In some embodiments of the present invention, Vcc is less than V_{FB} so that MOS-C 50 will be in the depletion mode and leakage will be reduced. This configuration may require special layout. MOS-C 50 has lower capacitance per unit area but with much lower leakage because of the depletion mode (there are fewer carriers to leak). It has good frequency response, but may have high series resistance. Note that the structure resembles the buried channel MOS transistor structure."

Add the following new paragraph following the paragraph ending at page 11, line 29:

--Some embodiments of the invention may include additional capacitors between the conductors carrying power supply and ground voltages, at least some of which are not in the depletion mode.--